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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/511,868	10/16/2004	Kwok Hong Luk	CN02 0008 US	8915
24738 7590 12/10/2007 PHILIPS ELECTRONICS NORTH AMERICA CORPORATION INTELLECTUAL PROPERTY & STANDARDS 370 W. TRIMBLE ROAD MS 91/MG SAN JOSE, CA 95131			EXAMINER MOON, SEOKYUN	
			ART UNIT 2629	PAPER NUMBER
			MAIL DATE 12/10/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

Application No.

10/511,868

Applicant(s)

LUK, KWOK HONG

Examiner

Seokyun Moon

Art Unit

2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 05 September 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1,2 and 6-13 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2 and 6-13 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 March 2007 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Remark*

1. Prior to the discussion regarding the Applicants' arguments, the Examiner respectfully submits that the subject matter of the instant Application might be different or distinguishable from the prior arts of record, but such subject matter is not presented and/or disclosed in the claims specifically enough to distinguish the instant invention from the prior arts of record.

### *Response to Arguments*

2. The Applicants' arguments filed on September 05, 2007 have been fully considered.

Regarding the rejection of claims 1 and 7,

The Applicants pointed out that the prior art of record (US 2001/0004257, herein after "Nitta") does not teach the claim limitation, "*means for providing said display parameters to an interface between the electronic apparatus and the display device*" [the Applicants' Remark: pg 6 lines 23-27].

Examiner respectfully disagrees.

As shown on fig. 2 of Nitta, the "DDC clock line 29" provides "DDC data" from the display electronics (the components shown on fig. 2 of Nitta, excluding "ASIC 21" and "receptacle 9") to the "receptacle 9". Then, the transmitted "DDC data" is passed to the computer through "receptacle 10", as shown on fig. 3 of Nitta. After receiving the "DDC data", the computer makes optimal settings for the display device and sends corresponding optimal data signals to the display device, and the optimal data signals are provided to "ASIC 21" through the "receptacle 9" [Nitta: par. (0015) lines 7-11]. Since the data/signal transfer between the display electronics and the display device is accomplished through the "receptacle 9" and "conversion cable 13", it would be reasonable to refer any of "receptacle 9" and the "conversion cable 13" as an interface between the display electronics and the display device.

The Applicants further pointed out that Nitta does not teach the claim limitation, “*a controller for selecting at least one application for the display device*”.

Examiner respectfully disagrees.

As explained in the previous Office Action, “*mux 31*” of Nitta selects one of two “*EDID*” according to the type of the interface. Since EDID is a type of data application, it would be reasonable to interpret EDID as an application.

Regarding the rejection of claim 6,

The Applicants' arguments are persuasive, and accordingly the previous rejection regarding claim 6 has been withdrawn. However, upon further consideration, different interpretation regarding the prior art is made.

Regarding the rejection of claim 8,

The Applicants pointed out, “*frequencies and frame rates may possibly be related to periods between gate select pulses and gate enabling pulses, but they are not the gate enable width, (e.g., the actual length of time that the gate is enabled*”.

However, the Examiner respectfully submits that the Applicants have failed to specify the meaning of the claim limitation, “*gate enable width*” or “*gate select width*” in the claim. As explained in the previous rejection, the Examiner interprets the claim limitation as the time period of how long it takes for each of the gates of the transistors included in the display panel to be enabled again after each of the gates of the transistors are enabled once.

Regarding the rejection of claim 9,

The Applicants pointed out that, in the prior art of record, the EDID is not provided from the electronic apparatus to the display device. The Applicants' arguments are persuasive, and accordingly the previous rejection regarding claim 9 has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made.

3. Prior to the rejections regarding the presented claims, the Examiner respectfully submits that claim 6 has been rejected under 35 U.S.C. 102(b) and 35 U.S.C. 103(a) based on different interpretations of the prior art of record, Nitta.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1, 2, 6, and 8** are rejected under 35 U.S.C. 102(b) as being anticipated by Nitta.

As to **claim 1**, Nitta teaches an electronic apparatus (the electronic components shown on fig. 2 excluding “ASIC 21” and “receptacle 9”) suitable for displaying information via a display device (a combination of “display screen” and “ASIC 21”) [par. (0029) lines 1-3], the display device having a display panel (“display screen”) provided with driving electronics (“ASIC 21”), the electronic apparatus comprising a controller (“multiplexer 31”) [fig. 2] for selecting at least one application (“EDID for the VGA interface” or “EDID for the DVI-I interface”) for the display device [par. (0031), emphasis on lines 4-5] and further comprising memory means (“memories 23 or 25”) for storing at least display parameters (the parameters included in “EDID for the VGA interface” or “EDID for the DVI-I interface”) related to the application and means (“DDC clock line 27” and “DDC data line 29”) for providing the display parameters to an interface between the electronic apparatus and the display device [fig. 2], the display parameters belonging to a group consisting of: a number of lines to be displayed (par. (0011) lines 4-8, note that resolution is referred to as a number of pixel columns by the number of pixel rows, thus the number of lines to be displayed is equivalent to the number of pixel rows), a number of columns to be displayed (par. (0011) lines 4-8, note that resolution is referred to as a number of pixel columns by the

number of pixel rows, thus the number of columns to be displayed is equivalent to the number of pixel columns), parameters ("*frequency of vertical scan signals*") related to driving transistors of the display device, and power saving parameters for the display device [par. (0011) lines 4-8 and par. (0052)].

As to **claim 2**, Nitta teaches the electronic apparatus further comprising memory means ("*memories 23 or 25*") [fig. 2] for storing parameters ("*EDID for the VGA interface*" or "*EDID for the DVI-I interface*") related to the selection of driving transistors [par. (0011) lines 4-8].

As to **claim 6**, Nitta teaches a display device (a combination of "*display screen*" and "*ASIC 21*") [par. (0029) lines 1-3] for use in an electronic apparatus (a combination of the electronic components shown on fig. 2 excluding "*ASIC 21*" and "*receptacle 9*", and "*display screen*") comprising a controller (a part of the "*multiplexer 31*" controlling the signal transmission from the lines "*B0*" or "*B1*" to the "*receptor 9*") [fig. 2] for selecting at least one application ("*EDID for the VGA interface*" or "*EDID for the DVI-I interface*") for the display device [par. (0031), emphasis on lines 4-5] and further comprising memory means ("*memories 23 or 25*") for storing at least display parameters (the parameters included in "*EDID for the VGA interface*" or "*EDID for the DVI-I interface*") related to the application and means ("*DDC clock line 27*" and "*DDC data line 29*") for providing the display parameters to an interface ("*receptor 9*") between the electronic apparatus and the display device [figs. 1 and 3], the display parameters belonging to a group consisting of: a number of lines to be displayed (par. (0011) lines 4-8, note that resolution is referred to as a number of pixel columns by the number of pixel rows, thus the number of lines to be displayed is equivalent to the number of pixel rows), a number of columns to be displayed (par. (0011) lines 4-8, note that resolution is referred to as a number of pixel columns by the number of pixel rows, thus the number of columns to be displayed is equivalent to the number of pixel columns), parameters ("*frequency of vertical scan signals*") related to driving transistors of the display device, and power saving parameters for the display device [par. (0011) lines 4-8 and par. (0052)], the display device comprising:

a display panel ("*display screen*") provided with driving electronics; and  
means (a part of the "*multiplexer 31*" controlling the signal transmission from the "*receptor 9*" to the lines "*A0*" or "*A1*") for recognizing an identification code at an interface between the electronic apparatus and the display device [pars. (0043) and (0049)].

As to **claim 8**, Nitta teaches the display parameters ("*frequency of vertical scan signals*" and "*frame rate*") [par. (0011) lines 4-8] including at least one of a gate select width, a gate enable width ("*frame rate*" and "*frequency of vertical scan signals*" indicates how long it takes for each of the gates of the transistors included in the display panel to be enabled again after each of the gates of the transistors are enabled once), and a power saving pulse width.

### ***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. **Claims 6 and 7** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nitta.

As to **claim 6**, Nitta teaches a display device ("*display 8*") [fig. 1] for use in an electronic apparatus comprising a controller (the CPU of the "*computer 1*") for selecting at least one application (various software applications installed in the "*computer 1*") for the display device and further comprising memory means (the memory of the computer, storing graphics or images related to the software applications) for storing at least display parameters related to the application and means (the output port of the "*computer 1*") for providing the display parameters to an interface between the electronic apparatus and the display device, the display device comprising:

a display panel provided with driving electronics; and  
means ("*multiplexer 31*") for recognizing identification code at an interface between the electronic apparatus and the display device [pars. (0043) and (0049)].

Nitta does not expressly teach the type of the display device.

However, Examiner takes Official Notice that it is well known in the art to use a LCD as a display device for an electronic apparatus.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the display device of Nitta to be LCD since LCD is well known for high native resolution and low power consumption.

Nitta as modified above teaches the display parameters belonging to a group consisting of a number of lines to be displayed, a number of columns to be displayed, parameters related to driving transistors of the display device, and power saving parameters for the display device (note that, in LCD, in order to display a graphic or an image, it is required to change either the amplitude of image signals or the time duration of providing image signals which are fed to the driving transistors).

As to **claim 7**, Nitta inherently teaches the driving electronics comprising storage means (such as buffers included in a data driver of a display panel) for storing a sequence of parameters controlling the panel received via the interface from the electronic apparatus since it is required for a data driver for a liquid crystal display to store graphic/image data signals temporarily (for example, for one horizontal scanning period or for one vertical scanning period) in order to display images or graphics corresponding to the received data signals, without any delay.

8. **Claims 1, 2, and 8-13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Moon (US 6,085,098).

As to **claim 1**, Moon [fig. 1] teaches an electronic apparatus suitable for displaying information via a display device, the display device having a display panel provided with driving electronics, the

electronic apparatus comprising a controller ("*processing circuit 26*") [fig. 2] for selecting at least one application (the various software applications shown on fig. 3) for the display device and further comprising memory means (the memory of the device storing the various software applications and/or the memory storing a vertical scanning or a horizontal scanning frequency of the display panel) for storing at least display parameters (graphics or images related to the software application and/or the vertical scanning frequency/the horizontal scanning frequency of the display panel, which are used for displaying graphical user interface of the software applications on the display panel) related to the application [col. 3 lines 63-65] and means (outputting means of the "*processing circuit 26*") for providing the display parameters to an interface (wires or connections between the display device and the electronic apparatus) between the electronic apparatus and the display device.

Moon does not expressly teach the type of the display device.

However, Examiner takes Official Notice that it is well known in the art to use a LCD as a display device for an electronic apparatus.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the display device of Moon to be LCD since LCD is well known for high native resolution and low power consumption.

Moon as modified above teaches the display parameters belonging to a group consisting of a number of lines to be displayed, a number of columns to be displayed, parameters related to driving transistors of the display device, and power saving parameters for the display device (note that, in LCD, in order to display a graphic or an image, it is required to change either the amplitude of image signals or the time duration of providing image signals which are fed to the driving transistors).

As to **claim 2**, Moon as modified above inherently teaches the electronic apparatus comprising memory means for storing parameters related to the selection of driving transistors since it is required for an electronic apparatus such as PDA, a cell phone, or a laptop, including a liquid crystal display to store a

vertical scanning frequency or a horizontal scanning frequency (which are related to the selection of driving transistors) in order to display images.

As to **claim 8**, Moon as modified above teaches the display parameters (the vertical scanning frequency or the horizontal scanning frequency, as discussed with respect to the rejection of claim 2) including at least one of a gate select width, a gate enable width (the vertical scanning frequency or the horizontal scanning frequency indicates how long it takes for each of the gates of the transistors included in the display panel to be enabled again after each of the gates of the transistors is enabled once), and a power saving pulse width.

As to **claim 9**, Moon teaches a method of an electronic apparatus [fig. 2] controlling a display device for at least one application (the various software applications shown on fig. 3), the method comprising:

programming into a memory of the electronic apparatus display parameters (the memory of the device storing the various software applications and/or the memory storing a vertical scanning or a horizontal scanning frequency required to drive a plurality of pixels included the display panel, in order to display images properly) related to the application [col. 3 lines 63-65]; and

providing the display parameters from the electronic apparatus to the display device ("22") [fig. 2].

Moon does not expressly teach the type of the display device.

However, Examiner takes Official Notice that it is well known in the art to use a LCD as a display device for an electronic apparatus.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the display device of Moon to be LCD since LCD is well known for high native resolution and low power consumption.

Moon as modified above teaches the display parameters belonging to a group consisting of a number of lines to be displayed, a number of columns to be displayed, parameters related to driving transistors of the display device, and power saving parameters for the display device (note that, in LCD, in order to display a graphic or an image, it is required to change either the amplitude of image signals or the time duration of providing image signals which are fed to the driving transistors).

As to **claim 10**, Moon teaches the method comprising storing the display parameters in a memory of the display device [col. 3 lines 63-65].

As to **claim 11**, Moon teaches the display parameters (the vertical scanning frequency or the horizontal scanning frequency) including at least one of a gate select width, a gate enable width (the vertical scanning frequency or the horizontal scanning frequency indicates how long it takes for each of the gates of the transistors included in the display panel to be enabled again after each of the gates of the transistors is enabled once), and a power saving pulse width.

As to **claim 12**, Moon [fig. 3] teaches the controller ("*processing circuit 26*") [fig. 2] being adapted to select the one application from a group of applications including both a telephone application ("*phone dial 52*") and a calculator application ("*calculator 48*").

As to **claim 13**, Moon teaches the application being one of a telephone application and a calculator application [fig. 3].

### ***Conclusion***

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Seokyun Moon whose telephone number is (571) 272-5552. The examiner can normally be reached on Mon - Fri (8:30 a.m. - 5:00 p.m.).

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (572) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

December 04, 2007

- s.m.

  
**SUMATI LEFKOWITZ**  
**SUPERVISORY PATENT EXAMINER**